

ABSTRACT OF THE DISCLOSURE

A register file for a data processing system comprises a memory unit, input ports, and output ports. The memory unit includes a plurality of memory locations. Each memory location is addressable by an encoded address, wherein the encoded address corresponds to at least one register and processor mode. The input ports receive inputs for addressing at least one memory location using an encoded address. The output ports output data from at least one memory location addressable by an encoded address.

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